Nanoindentation characterization of thin film stack structures by finite element analysis and experiments using acoustic emission testing

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A R T I C L E   I N F O

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Wafer testing
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A B S T R A C T

Increased risk of crack formation in the brittle insulating layers of crack-sensitive backend-of-line (BEOL) structures in semiconductor integrated circuits during wafer probing or wire bonding process is detrimental to product reliability. This paper describes the use of a high-resolution, in-situ material testing system that integrates acoustic emission (AE) testing with a nanoindentation system, as well as the finite element analysis (FEA) simulation method, for faster characterization of BEOL structures to optimize the reliability of wafer probing and wire bonding processes. This hybrid testing system is used to determine the critical load of thin film stack structures with Al-Cu input/output (I/O) pads, insulating layers, and the embedded Cu layers. Cracks were induced during the nanoindentation, and scanning electron microscopy (SEM) confirmed the formation and propagation of cracks in the insulating layers below the I/O pad. Finite element analysis (FEA) simulation was carried out to evaluate the contact-related stress distribution and obtain the critical stress by replicating the nanoindentation process to fully understand the critical conditions that lead to brittle fracture in insulating layers. Multiple thin film stack structures with different layer thicknesses are tested by experiment and correlated with simulation in parameter studies. We observed that as the thickness of the insulating layer increases and as the thickness of the embedded copper layer decreases, the critical loads will increase, which is in good agreement with previous studies. We also discovered that the critical loads of structures with thicker metal pads are not always higher than the thinner ones, which means the thicker metal pads do not certainly protect the structures better, as previous studies discovered.

1. Introduction

Bond pads in integrated circuits (ICs) are the metalized locations that undergo wafer probing and wire bonding, requiring physical contact between the metal pads and pointed probes or Cu wire [1,2]. During these processes, there exists an increased risk of crack formation in the dielectric layer directly beneath the pad, which can result in failure or higher reliability risk of the device due to short circuits or leakage. Numerous researchers have studied the SiO$_2$ layer failure in wafer bond pad structure by means of experimental [3–6] or simulation method [7–11]. However, there is a limited number of papers studying the insulating layer failure both by experiment and simulation [12]. In addition, the number of parameters studied in parameter analysis, e.g., influences of top metal thickness on critical loads, is only a small range.

To study the critical load that leads to the insulating layer failure of different structures, both experimental and simulation methods were utilized in this paper.

During wafer testing, contact between the probe and the sample is analogous to the nanoindentation process using a flat or a spherical tip if we assume an exclusively vertical movement of the probe tip. By convention, optical inspection of scanning electron microscopy (SEM) image cross sections, milled by focused ion beam (FIB), is used to detect and monitor the crack formation in the insulating layers after the indentaion process. However, optical imaging and FIB milling of the bond pad’s structure are destructive and not in real-time [13,14]. Acoustic emission (AE) testing has recently been developed as an attractive alternative that offers non-destructive, in-situ crack monitoring in multi-layer chip structures [15–17]. In brittle materials, like
In insulating layers, the AE phenomenon is associated with a sudden release of energy during crack formation. To generate and monitor cracks in the insulating layers, this work uses a sensor-indenter system, which consists of an AE sensor and an indenter with a flat diamond tip in a similar size of a real probe, as well as a nanoindentation system to enable a real-time, high-resolution indentation damage testing system. This paper is an extension of the work by Liu et al. [15] and Unterreithmeier et al. [16,17]. Our previous work mainly focused on the SiO$_2$-topped thin film stack structure to prove the feasibility of the experimental setup with AE testing. This paper studies a metal-topped thin film stack structure to study the critical load and critical stress of the samples with different thin film thicknesses. SEM images of FIB milled cross-sections are used to correlate the AE signals with different damage modes of multi-layer structures. Critical loads of structures with different film thicknesses are calculated and compared.

Experimentation alone is not sufficient to study insulation layer failure in metal-topped thin film stack structures because of the limitation of large test parameters of wafer structures due to the cost, resources, and lack of methods to obtain the critical stresses and deformation of testing samples. Therefore, the finite element analysis (FEA) simulation method is proposed to support the experimental study of thin film stack structures during the indentation process. Numerous researchers have studied the indentation process using the FEA method [18–20]. In this work, the indentation process was simulated using

![Diagram](image-url)
commercial FEA software (ANSYS). The stress distribution in the insulating layer of metal-topped thin film stack structures used in these experiments was obtained using FEA simulation. The effects of the indenter tip parameters (i.e., tip diameter and tip edge corner radius) and boundary conditions on the stress distribution and critical loads in FEA simulation are discussed. In addition, FEA simulation was used to explore beyond the range of variables covered in the experiments to study the layer thickness influences on critical loads and critical stress.

2. Materials and methods

2.1. Experimental test setup

The experimental test setup consists of a commercial nanoindentation system (iMicro KLA USA) and a customized sensor-indenter system [21], which was developed and patented by Infineon Technologies AG. A photo and a schematic drawing of the experimental setup are shown in Fig. 1 (a) and (b). A detailed description of the experimental setup used in this study has been published [15].

All tests were performed under constant loading rate control at the loading rate of 5 mN/s. The contact cycle is the same as the previous publication [15]. Each cycle started with a linearly increasing loading process until the maximum contact force was reached and ended with the unloading process until zero force was reached.

Fig. 2 (a) shows the schematic drawing of a thin film test structure of Wafer 22 and 10 μm flat tip. The tip is made of diamond with Young’s modulus of 1050 GPa. The backend-of-line (BEOL) structure generally has a metal layer deposited on top, and it includes contacts, insulating layers, and metal layers. The test structure was fabricated by Infineon on a silicon substrate. The following layers were deposited on a (1 0 0) silicon wafer in the following order: SiO2 (named SiO2-1), Ta (25 nm), Cu, Si3N4 (50 nm), SiO2 (named SiO2-2), Ta (50 nm), Ti (40 nm), and Al-Cu. Table 1 lists the film thickness of each layer in the eight test structures used in this study.

2.2. Failure analysis

To obtain the critical loads, Weibull analysis is used in this paper. Weibull analysis of experimentally derived AE test data is an effective method of determining the reliability of manufactured chips during product qualification using a relatively small amount of test data from the laboratory. Two-parameter Weibull distribution was used for reliability and failure distribution analysis in this paper. The failure probability density function and the cumulative failure distribution function of a two-parameter Weibull distribution are

$$f_x(x) = \frac{\beta}{\alpha x} \cdot \frac{x^{\beta-1}}{\alpha^\beta} \cdot e^{-\left(\frac{x}{\alpha}\right)^\beta}$$

and

$$F_x(x) = 1 - e^{-\left(\frac{x}{\alpha}\right)^\beta}$$

where $\alpha$ and $\beta$ are scale and shape parameters, respectively. The scale parameter, $\alpha$, is analog to the critical force, which is defined as the force corresponding to 0.63 cumulative failure probability. The shape parameter, $\beta$, is related to the scatter of the data. A higher $\beta$ value means a narrower distribution.

2.3. Finite element analysis

The indentation process was simulated using commercial FEA software (ANSYS). A 2D axisymmetric model was used to reduce the computation time [12]. Moreover, ideal isotropic bodies were assumed without considering the influence of microstructure and texture. The effect of the surface roughness of the top Al-Cu layer was also omitted. Surface roughness can affect nanoindentation results [18], but the surface roughness is much lower (typically less than 50 nm) than the indentation depths of several hundred nanometers used in this study. Therefore, the impact of roughness is assumed to be negligible in this work.

Fig. S1 shows the axisymmetric model and the boundary conditions of the tip and the multi-layer structure. The thickness of the silicon substrate is defined as 100 μm in this simulation. Fig. S2 supports that the differences between simulation results obtained from 100 μm and thicker silicon thickness are negligible. The width of the sample structure is 100 μm. Fig. S3 reveals that 100 μm is large enough to obtain the same result as a wider structure (150 μm). For the boundary conditions, force is applied on the top surface of a diamond indenter tip downwards in the vertical direction, and the bottom side of the silicon is fixed. The right side of the structure is set as a free surface. Fig. S3 also reveals that fixed support for the right side of the structure has little influence on the simulation results. Fig. 3 is a magnified image near the contact area composed of the sample structure and a flat diamond indenter tip with the 2D simulation mesh. The top pad (Al-Cu, Ti, and Ta layers) is considered as a whole layer with the same properties as the Al-Cu layer to simplify the simulation. The indenter tip has a conical shape with a 5 μm radius flat end and an opening angle of 60°. A fillet corner is created at the lower edge of the indenter tip with a radius of 1 μm to prevent stress singularities in the simulation. The influence of the radius of the fillet corner is studied in Fig. S4. The fillet corner radius affects the stress distribution of the Si3N4 layer. Thus, the fillet corner radius is fixed at 1 μm in all simulations. The interfaces between sample layers are perfectly bonded. The contact condition between the indenter tip and the structure surface has been studied in Fig. S5, which shows that the friction coefficient influences the stress distribution of the Si3N4 layer. Therefore, frictionless contact between the indenter and the structure surface was assumed in all simulations.

As shown in Fig. 3, refined meshes are created in and near the contact area to resolve the non-convergence problem during the simulation and

![Fig. 2](image-url)
to obtain an accurate solution. In contrast, coarser meshes are generated in the region far from the contact area to reduce the computation time. Further mesh refinement is implemented at the indenter tip corner and in the region where it potentially undergoes large deformation (the region near the tip corner at the upper surface of the Al-Cu layer). Quadratic meshes were constructed in brittle materials. Considering the non-linear properties and the large deformation of the ductile materials layer, especially the Al-Cu pad layer, triangle meshes are used in these layers to deal with the non-convergence issue.

The materials properties used in the simulation are given in Table 2. A bilinear stress-strain curve is used to describe the mechanical properties of ductile materials, i.e., Al-Cu, Ta, and Cu [7–9]. The tangent modulus of these ductile materials, which is the slope of the stress-strain curve stressed beyond the yield strength, is defined as 450 MPa. Fig. S6 shows an example of a bilinear stress-strain curve of Al-Cu materials. The brittle materials, i.e., SiO$_2$, Si$_3$N$_4$, and Si, have much higher yield strengths than the metal layers [22], and are treated as linear elastic materials.

3. Experiment results

3.1. SEM crack inspection after indentation

Fig. 4 shows SEM images of FIB cut cross-sections of the metal top structure (wafer 22) after loading with different maximum contact forces using a 10 µm flat tip. These SEM images reveal the crack formation processes and the failure mechanisms in the metal-topped stack structures. Cracks were observed in the SiO$_2$-1 layer and the Si$_3$N$_4$ layer, while no cracks were seen in the Cu layer, the SiO$_2$-2 layer, or the SiO$_2$-2/Si interface. The force-dependent failure mechanisms in the insulating layer of metal-topped structures involve: (1) the bottom-surface radial crack in the indentation contact area generated between 200 mN and 300 mN, marked by a red circle in Fig. 4 (b); and (2) the ring crack which penetrates through the whole insulating layer located outside of the contact area occurring between 450 mN and 500 mN, marked by a yellow circle in Fig. 4 (f).

The failure mechanisms of the metal-topped structure (wafer 22) are different from those exhibited in the insulating-topped structure after loading [15,17]. From SEM images of an insulating-topped test structure, published previously (Fig. S7) [15], three types of cracks on insulating layers are observed: (1) top-surface ring cracks outside of the contact area; (2) bottom-surface inner ring cracks in the contact area; and (3) bottom-surface radial cracks in the contact area. Fig. S8 is a schematic drawing of top views of crack evaluation of both metal-topped and insulating-topped top structures. From SEM images of the SiO$_2$-topped structure (380 nm SiO$_2$/700 nm Cu), the ring cracks were generated between 150 mN and 200 mN. The first crack of the metal-topped structure (wafer 22: 800 nm Al-Cu/380 nm SiO$_2$/700 nm Cu) is generated between 200 mN and 300 mN. We interpret these experimental results to mean that adding an extra metal layer on the brittle materials will reduce the stress concentration in brittle materials at the contact edge due to the metal plastic deformation; therefore, the critical load of the structure will increase.

3.2. Acoustic emission testing

Fig. 5 (a) is a representative plot of load vs. displacement (contact force vs. imprint depth) of wafer 22. The red asterisks represent the AE hits, and the relative size of each asterisk is proportional to the hit energy. These experiments were performed under controlled loads with a constant loading rate of 5 mN/s and maximum force of 600 mN using 10 µm flat tip. The turning point indicates the difference in the slope of the load-displacement curve between the low contact force (less than 70 mN) and the high contact force, which suggests the presence of nonlinear deformation processes. Significantly more AE signals were generated at lower contact force, and less occurrence of AE signals after the turning point is observed, which means that the AE hits before the turning point result from the plastic deformation of the metal top layer. Around 300 mN, one high-energy AE signal is generated, followed by a number of relatively small energy AE signals. This high-energy AE signal is due to the bottom-surface radial crack generated, verified by the SEM image in Fig. 4 (a) and (b). Fig. 4 (a) indicates there are no cracks in the insulation layer at a lower contact force, and Fig. 4 (b) shows the generated bottom-surface radial crack. The following small energy AE signals are most likely from the crack surface friction [15] and crack propagation. As the contact force increases, there is a discontinuity at 458 mN in the load-displacement curve in Fig. 5 (a). The discontinuity indicates the occurrence of a “pop-in” event, which usually correlates with fracture formation, crack initiation and growth, or the onset of plastic deformation [32]. Correspondingly, one high-energy AE signal is generated at 458 mN in Fig. 5 (a). In this study, the “pop-in” event is due to the failure of the insulating layer, i.e., ring cracks outside the indentation contact area, as shown in the SEM image in Fig. 4 (f).

Fig. 5 (b) is an example scatterplot of burst signal energy as a function of contact force of wafer 22. These data points are for all AE hits above the threshold derived from 100 repeat hits in a 10-by-10 array on each sample. The repeat indents were positioned 100 µm apart to avoid interference. At low force levels (below ~70 mN), a cluster of high-energy AE events is observed, which is due to the plastic deformation of the top metal layer. In addition to the SEM images of wafer 22 in Fig. 4, this conclusion is verified by comparing with AE scatterplots of SiO$_2$ top structure, which shows that there were no high-energy AE clusters at lower contact force as seen in Fig. S9 [15]. For wafer 22, the second cluster of AE signals is around 300 mN — this cluster is associated with the initial crack formation, which is verified by the SEM images in Fig. 4. Another cluster of high-energy AE signals happens around 470 mN, where the “pop-in” event occurs in the load-displacement curve. This cluster of AE signals results from the ring cracks formed in the SiO$_2$-1 layer, verified by the SEM images in Fig. 4. Fig. S10 (a-h) show the scatterplots of burst signal energy as a function of contact force of wafer 11 to wafer 88. The scatterplots of wafers 11, 55, and 66 (Fig. S10 (a), (e-f)) reveal that there are clusters of high energy signals at

<table>
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<th>Table 2: Materials properties used in FEA models.</th>
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<tr>
<td>Material</td>
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<tr>
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</tr>
<tr>
<td>Al-Cu</td>
</tr>
<tr>
<td>SiO$_2$</td>
</tr>
<tr>
<td>Si$_3$N$_4$</td>
</tr>
<tr>
<td>Cu</td>
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<tr>
<td>Si</td>
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a higher contact load, similar to the scatter plot of wafer 22 (Fig. 5 (b)). These AE signals represent the sudden penetration of the whole insulating layer by ring cracks. Another thing to note is that the first crack formations of wafers 55 and 77 are not as pronounced as the first crack formations of wafers 33 and 88. However, if AE hits and load-displacement curves of each indent are plotted as Fig. 5 (a), the first crack formation signals are indeed distinguishable from other AE signals, meaning that variances of the critical loads of these structures (wafer 55 and 77) are larger than other structures.
3.3. Critical load

Weibull distribution was used to calculate critical load of each wafer using the first AE signal of relatively higher energy occurring after plastic deformation. A cumulative probability of Weibull distribution as shown in Fig. S11. The critical force is analogue to the scale parameter, a. Table 3 displays the critical loads, and shape parameters, β, of different wafers, as well as their layer thicknesses. The shape parameter is related to the scatter of the data, and a higher value of β means a narrower distribution. The shape parameters of wafers 55 and 77 are relatively low, which is corresponding to the more scattered plots as shown in Fig. S10 (e) and (g). In contrast, wafers 33 and 88 have higher shape parameters and their critical load clusters are less spread.

4. Simulation results

Fig. 6 presents thin film deformation and the maximum principal stress of brittle materials layers (SiO₂, Si₃N₄, and Si) of wafer 22 at 294 mN (the critical load) using a 10 μm diameter flat tip. It is obvious that the soft Al-Cu layer has a pile-up effect because of the plastic deformation. The maximum principal stress distribution of brittle materials indicates that the insulating layer (SiO₂-1 and Si₃N₄ layer) is under tensile stress, and the highest stress is at the Si₃N₄ layer, as shown in Fig. 6. The inset of Fig. 6 shows the maximum principal stress distribution and normal stress distribution in three directions along the lower surface of Si₃N₄ (line A to B labeled in Fig. 6) at 294 mN; the x-axis represents the distance to the symmetry axis (point A in Fig. 6). In the contact area (distance less than 5 μm), the maximum principal stress is along the z-axis, which is perpendicular to the 2D x-y plane. The highest stress of the lower surface of Si₃N₄ layer is at the contact center with an amplitude of 7.79 GPa. The position of the highest stress is consistent with the position where radial cracks are first generated, as shown in the SEM images in Fig. 4 (b).

The stress distribution of the insulating layer at the critical force calculated from AE signals analysis is obtained. And critical stress is defined by the highest stress of the insulating layer. The crack initiation in brittle materials is different from classical fracture mechanics, which deals with the growth of pre-existing cracks. In brittle materials, finite fracture mechanics (FFM) assumes that cracks are formed instantaneously with finite size during indentation [33,34]. Following this convention, we assumed that the cracks in the insulating layer are initiated at both Si₃N₄ and SiO₂-1 layers spontaneously and instantaneously with finite size during indentation. Therefore, though the critical stress is obtained from Si₃N₄ layer, we consider the insulating layer as a whole.

Fig. 7 (a) plots the maximum principal stress in the Si₃N₄ layer vs. the contact load during the indentation simulation of wafers 22 and 33. The asterisk marks the critical load and the critical stress of each structure. The critical stress obtained from FEA also depends on the insulating layer thickness: Fig. 7 (b) shows the critical stress vs. the critical load of all wafer structures, and these data points are clustered by SiO₂ thickness. It reveals that the structures with higher SiO₂ thickness have relatively smaller critical stresses at the same force level. According to previous literature, the tensile strength of materials is expected to be higher for a thinner film in the general case [23]. The tensile strength will decrease as the SiO₂ thickness increases.

Table 4 presents the critical stress at the lower surface of the Si₃N₄ layer and the highest stress in the SiO₂-1 layer. Wafer 55 has the highest critical stress of 8.61 GPa, and wafer 33 has the lowest critical stress of 5.32 GPa. The reported tensile strength of bulk Si₃N₄ ceramic is 0.3751 GPa [35]. The critical stress obtained from the FEA simulation is much higher than this reported value. However, the tensile stress of Si₃N₄ depends on its thickness: the tensile stress of thin film materials is expected to be higher than the same materials in bulk form. Because in thinner materials, the density of dislocation is lower, and it is much more difficult to generate new dislocations. The reported strength of Si₃N₄ thin film is highly dependent on its thickness. In the field of microelectromechanical systems (MEMS), the fracture strength of Si₃N₄ increases to 1 GPa [36]. Edwards et al. [37] reported the fracture strength of around 5.87 GPa using 500 nm Si₃N₄ thin film. Kuhn et al. [38] obtained the strength of around 7 GPa with 450 nm thickness; Kaushik et al. [39] reported 5.5–7.1 GPa using 200–300 nm samples; Yoshiba et al. [40] published the strength of around 14.1 GPa using 100 nm specimen. The tensile stress of SiO₂ is also highly dependent on film thickness. Sharpe et al. [27] reported the value of around 0.364 GPa with 1000 nm thickness, Tsuchiya et al. [41], obtained that the mean strength is 1.2–1.0 GPa in a vacuum and 0.6–1.0 GPa in the air using 650 nm thickness specimen, and Hatty et al. [42] determined the fracture strength of 1000 nm SiO₂ thin film to be around 0.81 GPa. In addition to the sample thickness, the variations in these reported strengths are likely due to the sample’s width and length, different testing methods, or different microstructures of the specimen, which depend on the deposition method and processing parameters [35–42].

The critical stress of wafers 11 through 88 range from 5 GPa to 9 GPa. The reported fracture strength of Si₃N₄ discussed in the above paragraph, is also a wide range from 5 GPa to 14 GPa, depending on the sample’s size, testing method, or microstructure of the specimen [37–40]. And for the SiO₂ layer, the stress obtained from the simulation ranges from 0.8 GPa to 1.7 GPa, while the reported fracture strength of SiO₂ ranges from 0.3 GPa to 1 GPa. The simulated stress level in the Si₃N₄ layer is within range of reported strength; however, the simulated stress of the SiO₂ layer seems to be higher than the reported fracture strength. In the FFM framework, both the stress condition and the energy condition need to be fulfilled simultaneously, which means that the stress, as well as the released energy, must exceed critical values. Therefore, except for the discrepancies between the simulation and experiment, it is possible that the local stress level is higher than the fracture strength. The differences between the experiment and the simulation values may be attributed to a range of factors: the ideal assumption in the simulation, different thin film thicknesses, different contact conditions, or the different tip radius and tip fillet corner radius in the simulation vs. the experiment. The defined materials properties also affect the simulation results, as the mechanical properties of thin film structures vary with the deposition process and film thickness. For example, thinner layers have higher elastic modulus [23]. Considering these differences, the critical stresses of the Si₃N₄ and SiO₂ layers obtained at the critical load are in reasonable range of the reported fracture strengths. Though the simulation results are not able to give us exact values of critical stress, they are still meaningful for understanding the deformation of the structure and stress distribution in the insulating layers. The simulation is also useful in predicting trends in parameter studies.

<table>
<thead>
<tr>
<th>Table 3</th>
<th>Critical load calculated by AE signals and critical stress obtained from FEA simulation of different wafer structures.</th>
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<tbody>
<tr>
<td>Structure ID</td>
<td>Al-Cu (nm)</td>
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<tr>
<td>Wafer 11</td>
<td>800</td>
</tr>
<tr>
<td>Wafer 22</td>
<td>800</td>
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<tr>
<td>Wafer 33</td>
<td>800</td>
</tr>
<tr>
<td>Wafer 44</td>
<td>800</td>
</tr>
<tr>
<td>Wafer 55</td>
<td>1450</td>
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<tr>
<td>Wafer 66</td>
<td>1450</td>
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<tr>
<td>Wafer 77</td>
<td>1450</td>
</tr>
<tr>
<td>Wafer 88</td>
<td>1450</td>
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</table>
5. Parameter study

5.1. SiO$_2$-1 thickness effects

To study the effects of SiO$_2$-1 layer thickness on the wafer structure’s critical force, four wafer pair controls (11/22, 33/44, 55/66, and 77/88) were tested. In reference to Table 3, each pair are identical in BEOL structure except for thicknesses of their SiO$_2$-1 layer. The resulting critical forces of each wafer pair all show that larger SiO$_2$-1 layer thickness has the higher critical force.

To support the conclusion obtained from experiments, different SiO$_2$-1 thickness structures were simulated using FEA. Fig. 8 (a) shows the stress distribution of the lower surface of Si$_3$N$_4$ layer at 300 mN contact force. The thickness of the Al-Cu layer is 800 nm, and Cu layer is controlled at 700 nm. The results show that as the SiO$_2$-1 layer thickness increases, the highest stress will decrease.
which is consistent with the experiment results. These results can be explained by the beam bending theory: for a simple three-point bending case, the maximum stress of the bottom surface decreases as the beam thickness increases, and therefore, the critical force will increase.

5.2. Cu thickness effects

Cu layer thickness effects were studied in an identical manner, with wafer pairs 11/33, 22/44, 55/77, and 66/88. All wafer pairs gave the same conclusion that a thicker Cu layer results in a smaller critical force of the brittle, insulating layer. Different Cu thickness structures were simulated using FEA to support the experiment results. Fig. 8 (b) shows the stress distribution of the lower surface of the Si$_3$N$_4$ layer with different Cu thicknesses at 300 mN contact force. The thickness of the Al-Cu layer is 800 nm, and the SiO$_2$ layer is 380 nm. The simulations show that as Cu thickness increases, the highest stress will increase; therefore, the critical loads will decrease, which agrees with the experiment results. This result agrees with similar Cu layer thickness studies in the literature [9–17]. An intuitive explanation of this phenomenon is that as the thickness of the Cu layer increases, the displacement of the upper surface of the Cu layer will increase, causing higher bending deformation of the upper insulating layer, which will result in higher bending stress at the insulating layer surface.

5.3. SiO$_2$-2 thickness effects

The influence of SiO$_2$-2 layer thickness was only studied by FEA simulation. Fig. 8 (c) shows the stress distribution of the lower surface of the Si$_3$N$_4$ layer with different SiO$_2$-2 thicknesses at 300 mN contact force. The thickness of the Al-Cu layer is 800 nm, the SiO$_2$-1 layer is 380 nm, and the Cu layer is 700 nm. The simulations results show that the SiO$_2$-2 layer does not influence the stress distribution as much as other layers in this structure.

5.4. Al-Cu thickness effects

The Al-Cu layer thickness effect was experimentally studied with the method used for the SiO$_2$-1 and Cu layer thickness effect studies, with wafer pairs 11/66, 22/55, 33/88, and 44/77. Wafers 77 and 88 have larger SiO$_2$-2 layer thicknesses of 2040 nm, compared to 1740 nm (Table 3), but the simulation results in section 5.3 indicate that higher SiO$_2$-2 layer thickness results in negligible stress in the brittle insulating layer (Fig. 8 (c)). With that said, any difference in critical load in this

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Table 4

<table>
<thead>
<tr>
<th>Experiment</th>
<th>FEA Simulation</th>
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<tr>
<td></td>
<td>Critical Load (mN)</td>
<td>Critical Stress in Si$_3$N$_4$ (GPa)</td>
</tr>
<tr>
<td>Wafer 11</td>
<td>332</td>
<td>6.32</td>
</tr>
<tr>
<td>Wafer 22</td>
<td>294</td>
<td>7.79</td>
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<tr>
<td>Wafer 33</td>
<td>409</td>
<td>5.32</td>
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<tr>
<td>Wafer 44</td>
<td>389</td>
<td>6.78</td>
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<td>Wafer 55</td>
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<td>8.61</td>
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<tr>
<td>Wafer 66</td>
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<tr>
<td>Wafer 77</td>
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<td>7.80</td>
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<tr>
<td>Wafer 88</td>
<td>379</td>
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Fig. 8. (a) SiO$_2$-1, (b) Cu, and (c) SiO$_2$-2 thickness influence on stress distribution of the lower surface of Si$_3$N$_4$ at 300 mN contact force.
comparison can be confidently attributed to exclusively the difference in Al-Cu layer thickness. When comparing the critical load values of these wafer pairs (Table 3), it is clear that larger Al-Cu layer thickness results in a smaller critical load.

To thoroughly study the Al-Cu thickness influence, varying Al-Cu thickness structures were modeled and compared by FEA simulation. The simulations used the following layer thicknesses: 380 nm of SiO$_2$-1, 700 nm of Cu, and 540 nm of SiO$_2$-2. Fig. 9 (a) shows the contact force vs. 10 μm flat tip imprint depth curve of different Al-Cu thicknesses. The structure first undergoes the linear deformation at a lower contact force (less than 70 mN), followed by the non-linear deformation. At the same contact force, thicker metal layers have greater imprint depth. In the non-linear deformation region, as the contact force increases, the slope of the force-depth curve becomes larger, which means the stiffness of the samples increase, and the sample becomes harder to penetrate. Fig. 9 (b) shows the curve of contact force vs. displacement of the central point of the upper surface of SiO$_2$-1 (point C in Fig. 6). It reveals that the deformation of the insulating layers of the varying Al-Cu thickness structures is similar at the same contact force. It suggests that the difference in the imprint depth results from the difference in the deformation of the Al-Cu layer. Fig. 9 (c) plots the relative remnant metal layer thickness (remnant thickness divided by original thickness) vs. metal layer thickness at 300 mN contact force. This plot clearly shows that thicker Al-Cu layers are more easily compressed than thinner ones, which in agreement with other simulation work [10] and experiments [6].

A range of Al-Cu layer thicknesses were further analyzed at different maximum contact forces. Fig. 10 (a), (c), and (e) show the stress distribution along the lower surface of the Si$_3$N$_4$ layer at different maximum contact forces (50, 100, and 300 mN, respectively). Fig. 10 (b), (d), and (f) show how the highest maximum principal stress of the Si$_3$N$_4$ layer changes with Al-Cu thickness at different maximum contact forces (50, 100, and 300 mN, respectively). At 50 mN contact force, the Al-Cu layer is under linear deformation (Fig. 9 (a)). The position of the highest stress of all Al-Cu layer thicknesses is near the contact edge (5 μm), and as the Al-Cu thickness increases, the highest stress decreases, and the position of the highest stress moves toward the symmetry axis. Therefore, at a lower contact force where the metal pad is only under elastic deformation, higher metal top layer thickness prevents stress concentration and protects the structure better. As seen in Fig. 10 (c), as the layer thickness increases, the position of the highest stress moves toward the symmetry axis. At 300 mN, except for the 300 nm structure, the position of the highest stress is near the symmetry axis, as displayed in Fig. 10 (e), and the highest stress increases first and then decreases slightly at 2700 nm as shown in Fig. 10 (f). To conclude, at lower contact force, the stress decreases as thickness increases monotonically, while at higher contact force, the influences of the Al-Cu thickness are non-linear because of the nonlinear properties of the metal. At higher contact force, the highest stress will increase as thickness increases, but undergoes a slight decrease at around 2700 nm. The simulation result is consistent with our experiment results for the 800 nm and 1450 nm structures, which shows that the thicker Al-Cu structure has a smaller critical load.

Other researchers have studied the metal top layer thickness effects during the wire bonding process or wafer testing by experiment [6] and simulation [7,8]. Their results show that thicker metal pads reduce the probabilities of brittle layer failure, which seems to be contradictory to this study’s observation. To explain the discrepancy between our conclusion and other researchers’ observation, we found that the stress distribution at the same contact force was compared in this study, while the same displacement was applied in other works [6-8]. Therefore, to
compare with other studies more accurately, we present Fig. 11 (a) and (c) which show the stress distribution of the lower surface of the Si$_3$N$_4$ layer vs. the distance to the contact center at an imprint depth of 0.1, and 0.3 $\mu$m, respectively. Fig. 11 (b) and (d) plot the highest stress of the lower surface of the Si$_3$N$_4$ layer vs. Al-Cu thickness at an imprint depth of 0.1, and 0.3 $\mu$m, respectively. These imprint depth values were selected because at 0.1 $\mu$m imprint depth, structures were under elastic deformation, and at 0.3 $\mu$m imprint depth, they were under plastic deformation. In both cases, as Al-Cu layer thickness increases, the highest stress decreases, meaning there is a lower probability of brittle layer failure. In conclusion, if imprint depth is controlled, a thicker layer of Al-Cu will lead to fewer stresses in the insulation layer, and if contact force is controlled, the circumstance becomes more complex and it depends on the contact force.

6. Conclusions

AE testing has been utilized to determine the critical load of crack-sensitive BEOL structures used in semiconductor integrated circuit fabrication upon nanoindentation with a flat diamond tip. SEM imaging was used to visually confirm the formation and propagation of cracks. Bottom-surface radial cracks were observed first, at lower contact load. Ring cracks that penetrate through the whole insulating layer outside the contact area were observed second, generated at high contact load. The critical loads of wafers with different thin film layer thicknesses were obtained by analyzing the acoustic emission (AE) signals associated with specific crack formation.

In addition to the experimental-based crack analysis, FEA simulation was performed to evaluate the stress distribution and critical stress to fully understand the critical conditions that lead to brittle fracture in insulating layers. Considering the differences between the experiment and the simulation, the critical stresses of the Si$_3$N$_4$ layer obtained at the
critical load is in a reasonable range of the reported fracture strength. The simulation also qualitatively supports that the critical stress depends on the thickness of the insulating layer. Multiple thin film stack structures with different layer thicknesses were tested by experiment and simulation for parameters studies. The influences of the first insulating layer, SiO$_2$-1, and the Cu layer embedded below the first insulating layer were investigated both by experiment and simulation, with resulting values in good agreement with previous studies—i.e., the thicker the insulation layer, the higher the critical load; and the thicker the Cu layer, the lower the critical load. The effect of thickness of the top metal pad was studied systematically. In the experiment of 800 nm and 1450 nm Al-Cu top structure, higher Al-Cu thickness leads to a lower critical load. From the simulation results, it can be noted that if the imprint depth is controlled, a thicker Al-Cu layer will result in fewer stresses in the insulation layer as previous studies have reported. In comparison, if contact force is controlled, the circumstances become more complex: at lower contact force, the stress decreases as thickness increases monotonically; while at higher contact force, because of the nonlinear properties of the metal, in general, the stress will increase as thickness increases; therefore, the critical load will decrease as thickness increases.

CRediT authorship contribution statement

Chen Liu: Writing – review & editing, Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. Oliver Nagler: Writing – review & editing, Supervision, Resources, Project administration, Methodology, Conceptualization. Florian Tremmel: Writing – review & editing, Software, Data curation. Marianne Untereitmeier: Writing – review & editing, Resources, Methodology, Conceptualization. Jessica J. Frick: Writing – review & editing. X. Wendy Gu: Writing – review & editing, Supervision, Resources. Debbie G. Senesky: Writing – review & editing, Supervision, Resources, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mssp.2022.106737.

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